IN THE CLAIMS

1-3. (Cancelled).

4. (Currently Amended) An array panel comprising:

a substrate including a gate driver region, a data pad region, and a storage capacitor region;

a ~~gate~~ first conductive line formed in the data pad region ~~extended on the substrate in a first direction~~;

a ~~data~~ second conductive line formed in the storage capacitor region ~~extended on the substrate in a second direction~~, a portion of the second conductive line functioning as a capacitor electrode of a storage capacitor;

a first switching element ~~including a gate electrode, a source electrode, and a drain electrode, the switching element being~~ formed in a pixel region ~~defined by the gate and the data lines~~;

~~a photoelectric cell for generating electrons in proportion with the intensity of light supplied from outside, thereby generating an electrical signal;~~

a first transparent layer including first and second transparent electrodes formed on the first and second conductive lines, respectively;

an insulating layer having a first contact hole extending to the first transparent electrode on the first conductive line in the data pad region and a second contact hole extending to a drain electrode of the first switching element in the pixel region;

an organic layer formed on the insulating layer, the organic layer having a first removed portion exposing the first transparent electrode in the data pad region and a second removed portion exposing the drain electrode of the first switching element in the pixel region; and

a second transparent layer formed on the organic layer, the second transparent layer including a third transparent electrode directly connected to the first transparent electrode through the first contact hole in the data pad region and a fourth transparent electrode directly connected to the drain electrode through the second contact hole in the pixel region,

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wherein a portion of the organic layer in the storage capacitor region is removed, and the fourth transparent electrode extends to the storage capacitor region to be disposed directly on the insulating layer in the storage capacitor region, thereby forming the storage capacitor comprising the capacitor electrode, the second transparent electrode, a portion of the insulating layer in the storage capacitor region, and the fourth transparent electrode extending to the storage capacitor region.

~~a pixel electrode formed in the pixel region, the pixel electrode gathering electrons generated from the photoelectric cell;~~

~~a storage capacitor formed in the pixel region, the storage capacitor storing the electrons gathered by the pixel electrode, wherein the storage capacitor comprises a capacitor electrode, a first electrode formed directly on the capacitor electrode, an insulating layer, and the pixel electrode formed directly on the insulating layer;~~

~~a gate driver making an electrical contact with an end portion of the gate line on the substrate, the gate driver sequentially providing a scan signal for driving the switching element; and~~

~~a data pad making an electrical contact with an end portion of the data line on the substrate, the electrons stored in the storage capacitor being extracted to the data pad through the switching element in case that the switching element is turned on.~~

5. (Currently Amended) The array panel of claim 4, further comprising a gate driver formed in the gate driver region, wherein the gate driver includes a plurality of stages sequentially making an electrical contact with each other, each stage including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, so that the stages function as a shift register.

6-7. (Cancelled).

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8. (Currently Amended) The array panel of claim 4, wherein at least one of the first, second, third and fourth transparent ~~pixel~~ electrodes comprises indium tin oxide (ITO).

9. (Currently Amended) The array panel of claim 4, wherein the fourth transparent ~~pixel~~ electrode covers ~~is disposed on~~ a whole ~~surface~~ of the first switching element in the pixel region.

10. (Currently Amended) The array panel of claim 4, further comprising a second switching element in the gate driver region, wherein the second transparent layer further includes a transparent pattern ~~pixel electrode is~~ disposed on a portion of the organic layer in the gate driver region to cover a whole ~~surface~~ of the second switching element in the gate driver region.

11. (Currently Amended) A method of manufacturing an array panel, the method comprising:

forming a first switching element in a pixel region, ~~and~~ a second switching elements in a gate driver region, a first conductive line ~~for~~ in a data pad region and a second conductive line ~~for~~ in a storage capacitor region, wherein a portion of the second conductive line functions as a capacitor electrode of a storage capacitor~~, the first switching element corresponding to a pixel region of a substrate~~;

forming a first transparent layer ~~electrode~~ on the first and second conductive lines to form first and second transparent electrodes on the first and second conductive lines, respectively;

sequentially coating an insulating layer and an organic layer ~~on~~ to cover the first and second transparent electrodes, and to cover the first and second switching elements;

exposing a portion of the organic layer to light and developing the organic layer to ~~partially removing~~ remove a portion of the organic layer over the first transparent electrode ~~corresponding to the first and second conductive lines~~ and a portion of the organic layer over a drain electrode of the first switching element ~~by exposing to light~~, and to remove a portion of the organic layer in the storage capacitor region;

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~~partially~~ removing a portion of the insulating layer to form a first contact hole extending to the first transparent electrode on the first conductive line ~~of the data pad~~ and form a second contact hole extending to the drain electrode of the first switching element; and

forming a second transparent layer on the organic layer, and patterning the second transparent layer to form a ~~electrode for collecting electrons, the second~~ third transparent electrode ~~being~~ directly connected to the first transparent electrode in ~~of~~ the data pad region and form a fourth transparent electrode directly connected to the drain electrode, wherein the fourth ~~second~~ transparent electrode extends to the storage capacitor region to be disposed directly ~~corresponding to the second conductive line is formed~~ on the insulating layer in the storage capacitor region, thereby forming the storage capacitor comprising the capacitor electrode, the second transparent electrode, a portion of the insulating layer in the storage capacitor region, and the fourth transparent electrode extending to the storage capacitor region ~~between the second transparent electrode and the second conductive line~~.

12. (Currently Amended) The method of claim 11, further comprising:

forming a protecting layer on the ~~exposed~~ organic layer and the patterned second transparent layer ~~electrode~~;

forming a light conductive semiconductor layer on the protecting layer; and

forming an electrode on the light conductive semiconductor layer.

13. (Currently Amended) The method of claim 11, wherein the fourth ~~second~~ transparent electrode covers ~~is disposed on~~ a whole ~~surface~~ of the first switching element.

14. (Currently Amended) The method of claim 11, wherein the second transparent layer ~~electrode is disposed on~~ is patterned to be disposed on a portion of the organic layer in the gate driver region and to cover a whole ~~surface~~ of the second switching element.

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15. (Previously Presented) The method of claim 11, wherein the second switching element is a plurality of thin film transistors comprising amorphous silicon, said plurality of

thin film transistors arranged in a plurality of stages sequentially making an electrical contact with each other, and each stage including an input terminal and an output terminal through which corresponding signals are transmitted, a start signal being transmitted to the input terminal of a first stage, and an output signal of each stage being sequentially outputted from each output terminal, so that the stages function as a shift register.

16. (New) The array panel of claim 4, further comprising a photoelectric cell for generating electrons in proportion with the intensity of light supplied from outside, thereby generating an electrical signal.

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